Amendments to the Claims

1. (CURRENTLY AMENDED) A microcontroller, wherein the microcontroller ~~(10)~~ has at least one status bit ~~(12)~~ by means of which a writing and/or reading of N-bit address words by at least one standard instruction of the microcontroller ~~(10)~~ can be forced, wherein the address length N of the N-bit address word is greater than the address length of a standard set of instructions or of equivalents of other sets of instructions of the microcontroller.

2. (ORIGINAL) A microcontroller as claimed in claim 1, characterized in that the address length N of the N-bit address word is greater than 16.

3. (ORIGINAL) A microcontroller as claimed in claim 2, characterized in that the address length N of the N-bit address word has the value 20, 24 or 32.

4. (CURRENTLY AMENDED) A microcontroller as claimed in ~~any of the preceding claims~~claim 1, characterized in that the at least one standard instruction is an LCALL, ACALL or RET instruction or the like.

5. (CURRENTLY AMENDED) A microcontroller as claimed in ~~any of the preceding claims~~claim 1, characterized in that the at least one status bit ~~(12)~~ can be set and/or deleted by means of at least one computer-readable storage medium ~~(14)~~.

6. (CURRENTLY AMENDED) A microcontroller as claimed in ~~any of the preceding claims~~claim 1, characterized in that the at least one status bit ~~(12)~~ is part of at least one Special Function Register ~~(16)~~.

7. (CURRENTLY AMENDED) A microcontroller as claimed in ~~any of the preceding claims~~claim 1, characterized in that the at least one status bit ~~(12)~~ is implemented in the hardware of the microcontroller ~~(10)~~.

8. (CURRENTLY AMENDED) A microcontroller as claimed in ~~any of the preceding claims~~claim 1, characterized by a design for use in a smartcard.

9. (CURRENTLY AMENDED) An addressing method, characterized in that at least one status bit ~~(12)~~ of a microcontroller ~~(10)~~ is set and as a result a writing and/or reading of N-bit address words by means of at least one standard instruction of the microcontroller ~~(10)~~ is forced.

10. (ORIGINAL) A method as claimed in claim 9, characterized in that the at least one standard instruction is an LCALL, ACALL or RET instruction or the like.

11. (CURRENTLY AMENDED) A method as claimed in ~~either of claims 9 and 10~~claim 9, characterized in that the at least one status bit ~~(12)~~ is set and/or deleted by means of at least one computer-readable storage medium ~~(14)~~.

12. (CURRENTLY AMENDED) A method as claimed in ~~any of claims 9 to 11~~claim 9, characterized in that the at least one status bit ~~(12)~~ is part of at least one Special Function Register ~~(16)~~.

13. (CURRENTLY AMENDED) A method as claimed in any of claims 9 to 12, characterized in that the at least one status bit ~~(12)~~ is implemented in the hardware of the microcontroller ~~(10)~~.